EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven M. Santisi, Reg. No. 40,157 on 08/11/2008.

The application has been amended as follows:

Claim 1 (Currently Amended): A method of determining in which of n intervals a sum of two or more numbers resides comprising:

determining the two or more numbers; and

providing fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

employing the fewer than n compress circuits to determine in which of the n intervals the sum of the two or more numbers resides,

wherein a result of a floating point computation in a processor is determined based on the determination of which of the n intervals the sum of the two or more numbers resides,

wherein the providing results in less physical space used than if n compress circuits were provided.

Claim 11 (Currently Amended): An apparatus for use in determining in which of n intervals a sum of two or more numbers resides comprising:

fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

a plurality of sign check circuits coupled to the compress circuits, the sign check circuits adapted to generate a sign check bit that corresponds to each of the n intervals based on the two or more outputs generated by the compress circuits,

wherein a result of a floating point computation in a processor is determinable ~~may be determined~~ based on the sign check bits,

wherein the providing results in less physical space used than if n compress circuits were provided.

Claim 21 (Currently Amended): A method of determining in which of n intervals a sum of two or more numbers resides comprising:

determining the two or more numbers; and

providing fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

employing the fewer than n compress circuits to determine in which of the n intervals the sum of the two or more numbers resides by:

generating carry and sum bits based on the two or more numbers and range information;

selectively providing the carry and sum bits to a plurality of sign check circuits;

determining a sign check bit for each interval based on the selectively provided bits; and

determining in which interval the sum resides based on the sign check bit for one or more of the intervals,

wherein a result of a floating point computation in a processor is determined based on the determination of in which interval the sum resides,

wherein the providing results in less physical space used than if n compress circuits were provided.

Claim 22 (Currently Amended): An apparatus for use in determining in which of n intervals a sum of two or more numbers resides comprising:

fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into a carry vector and a sum vector;

a plurality of sign check circuits coupled to the compress circuits, the sign check circuits adapted to generate a sign check bit that corresponds to each of the n intervals based on the carry and sum vectors generated by the compress circuits; and

a plurality of signal paths adapted to selectively route bits of the carry and sum vectors of each compress circuit to the plurality of sign check circuits,

wherein a result of a floating point computation in a processor is determinable ~~may be determined~~ based on the sign check bits,

wherein the providing results in less physical space used than if n compress circuits were provided.

Claim 25 (Cancelled).

Allowable Subject Matter

2. Claims 1-24 are allowed.

3. Claim 25 is cancelled.

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a method and apparatus of determining in which of n intervals a sum of two or more numbers resides comprising: providing fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to: input the two or more numbers; input range information regarding ranges used to define the n intervals; and compress the two or more numbers and the range information into two or more outputs; and employing the fewer than n compress circuits to determine in which of the n intervals the sum of the two or more numbers resides along with other limitations as clearly cited in independent claims 1, 11 and 20-21.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 7:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

August 12, 2008